An Optimization of ALU using Reversible Logic Gate

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***Abstract*—This research proposes a new method for designing arithmetic logic units that make use of reversible logic. For a long time, scientists have been trying to improve methods for reducing energy consumption. It has been discovered that reversible logic can be a viable option for improving efficiency. Mathematical calculations, including addition, subtraction, and many logical operations, are commonly performed on digital calculators. Here, we propose a novel approach to computing by employing reversible logic to generate the results of many arithmetic and logical operations in a single line. Two methods of addition are used to create the ALU presented in this research; first, FPGA is used to verify the procedure, and then reversible logic is employed for building an optimized arithmetic and logic unit. Using Xilinx Vivado 2018-1, the concept was evaluated in the Artix-7 series. The conclusions of the study indicate a reduction of 50% in the number of ancillary inputs, 40% in garbage output, and 75% in propagation latency.**

***Keywords*— Garbage Output; Logical computations; Reversible logic; Quantum cost; Gate count; Field Programmable Gate Array; Verilog HDL**

I. INTRODUCTION

The interminable requirements of high speed, area efficient, and low power data path systems are incorporated in CMOS VLSI design. Numerous technologies and tools have evolved to achieve the tradeoff between measurable performance parameters. Conventionally, digital circuit design is approached by irreversible logic gates. Whenever there are fewer outputs than inputs, information is lost. Landauer[1] found that digital circuit bit losses cost KTln2, where K is the "Boltzmann constant" and T is the computer's operating "temperature". He also demonstrated that the energy cost of computing is limited to those actions that are logically irreversible. Based on this approach, Bennett [2] demonstrated that employing reversible circuitry to perform calculations prevents these energy losses. Energy loss owing to the Landauer limit is crucial because heat generation will likely grow, causing information loss. Preserving data is a driving force behind reversible computing studies. Additionally, quantum computing which is the futuristic computing paradigm inherently uses reversible computing, circuits should be built using reversible logic gates. This article attempts to construct a unique optimized efficient ALU.

Because of its piecewise linear mapping across input and output, reversible logic has minimal power dissipation throughout computing. The gates needed to make reversible logic circuits are well-defined. When trying to determine the optimal configuration for a reversible logic circuit, it's important to think about quantum cost (QC), constant input (CI), garbage output (GO), and logical computation. One key to improving performance metrics is the ability to synthesise reversible circuits. Reversible circuit design complexity is contrasted in terms of quantum cost, the number of primitive quantum gates needed to construct the circuit, and garbage outputs, the end outputs that are not used as primary outputs.

Quantum computers use reversible logic extensively. A quantum computer is a quantum network of quantum logic gates that execute elementary unitary operations on one, two, or more qubits. The traditional bit values 0 and 1 can represent every elementary unit of information as a qubit. Reversible logic gates are required while designing such circuits. Reversible gates are logic gates with a 1:1 mapping between their inputs and their outputs. When it comes to the idea and design of circuits for electrical devices, CMOS technology is crucial. Physical limitations make it difficult, if not impossible, to design small-scale circuits utilising CMOS technology. To be effective as an ALU, a reversible gate must be able to increase the variety of logical operations it can compute while simultaneously minimising the number of select lines and logical output lines, along with cost and latency.

To guarantee that these logic gates are designed with reversibility in consideration, we present two theorems.

Theorem 1: A perfect j-input, j-output programmed reversible logic gate contains m-fixed select inputs, n-fixed select outputs, d-data inputs, and p-propagated outputs, $|d - p| = |m - n|$.

Both "d - p" and "m - n" must have the same value for there to reduce ancilla inputs.

Theorem 2: If the m select inputs are programmed to a programmable reversible logic gate, then can do at most "$n * 2^m$" logical operations.

In the remaining portions of the article, we will cover: Theory behind reversible logic, such as its reversible gates and performance measurements, is discussed in Section 2.

Before discussing the proposed model in Section 4, Section 3 provides a description of the existing approaches. Thereafter, the findings and in-depth analysis are presented in Section 5. Future scopes are included in the conclusion.

II. BACKGROUND

Traditional logic's Boolean functions have an inefficient input-to-output mapping, leading to wasted energy and data while processing [3]. Reversible logic technology maps input and output uniquely [4]. Many emerging fields, including digital signal processing, DNA computing, artificial neural networks, image processing, quantum cryptography, and nanotechnology, provide promising applications for reversible logic.

A. Reversible Logic

In contrast to conventional logic gates like AND, OR, XOR, NAND, and NOR, which have many inputs but only one output, reversible logic gates contain two sets of inputs and one set of outputs. Reversible logic gates provide piecewise linear input-output translations. A reversible logic circuit is a type of logic circuit that can be reversed once it has been built [5]. Cascading of the reversible gates is carried out resulting in the desired reversible logic circuit.

B. Reversible Gates

A significant factor that deviates reversible logic away from conventional logic is the retracing of the inputs from the output. Commonly used gates in reversible circuit design are Feynman [5], Fredkin [6], Toffoli [7], HNG [8], and Peres gate. To achieve desired functionality additional inputs may be added to make a reversible function bijective and it will be maintained at a constant value '0' or '1', hence they are called constant inputs/Ancilla input [9]. Feynman gates, Fredkin gates, and HNG gates, all of which are reversible, are discussed and illustrated below.

1) Feynman Gate

Primitive gate whose size is 2*2, having input Iv(a, b) having mapped to output through, where p and q are outputs. This gate is also commonly referred to as CNOT gate. Copying operation required in the circuit design is accomplished through CNOT gate. Quantum cost of any circuitry is estimated depending on quantity such gates deployed. Quantum cost of CNOT gate is 1. Fig.1 shows a Feynman gate schematic and its logical equation.

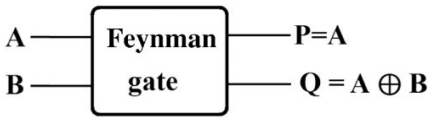

Fig.1. Schematic of a Feynman Gate

2) Fredkin Gate

Fredkin Gate is a 3*3 gate having input Iv(a, b, c) and mapping with the output combination of p=a ,q= ¯(a) b xor ac with a quantum cost of 5. It finds application in circuit design requiring AND, OR/ XOR operations. Schematic and truth table of Schematic along with logical equations are given in Fig. 2.

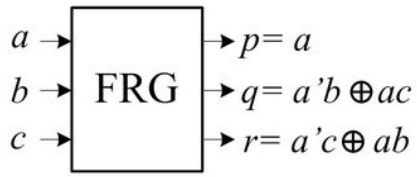

Fig.2. Schematic of a Fredkin gate

3) HNG Gate

Four-by-four reversible gate that functions as a complete adder when used alone. Input "a, b, c, d" have the relation to the output through, and if d input is maintained at a constant value of 0, then full adder is realized. HNG gate provides logical operations at quantum cost of 6. Fig. 3 show the HNG gate's schematic and logical expression.

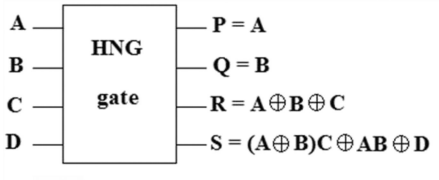

Fig. 3. Schematic of an HNG gate

C. Performance Parameters

Reversible logic circuit efficiency is optimized by constant/ancillary inputs (AI), garbage outputs, quantum cost, delay, and computational complexity. In certain cases, number operations and gate count may be used to analyze the circuits. Add up the number of primitive gates (1*1 and 2*2 gates) necessary to build a reversible circuit to calculate its quantum cost (QC) [7]. Realization of the desired circuit results in a number of outputs that are unwanted for further processing, such outputs are labelled as garbage output (GO), for the proper synthesis of circuits this must be least minimum or zero. A number of reversible gates employed for design determines the logical depth and ultimately the delay involved [8]. The most important criteria one should be aware of is reversible logic does not support fan-in and feedback in circuits. Calculation of Garbage Output is:

The count of the Primary inputs is given as:

$$P.I.(n) = (3+2xn+1) = (2n+4) \quad (1)$$

The number of ancillary inputs is given as:

$$A.I.(n) = 2n-1 \quad (2)$$

Number of primary outputs is:

$$P.O.(n) = n+1 \quad (3)$$

As a result, the sum of garbage output produced is:

$$G.O(n) = P.I.(n) + A.I.(n) - P.O.(n) \quad (4)$$

Substituting and solving Eq. 1, 2, 3 in Eq. 4 gives Total Garbage output for the proposed design as:

$$G.O(n) = 2n+4+2n-1-n-1 = (3n+2) \quad (5)$$

Garbage outputs are the results of calculations that aren't used as the main output or as input to another gate. These are crucial to achieving reversibility and so can't be avoided.

D. Motivation for the Research

Devices need reversible computing to become more portable once more. In turn, this will allow circuit element sizes to shrink to atomic levels, making portable devices a possibility. In spite of the impending high prices of hardware design, reversible computing is essential in the modern computer era because power costs and performance are more important than logic hardware costs.

III. EXISTING WORK

ALU designs using reversible logic have been attempted by several researchers and their interest to build the better

performing ALU has led to the invent of different approaches to design the ALU converging to achieve the optimization and flexibility of the operations. Among the available architecture in the literature the categorization of the ALU can be made as - dedicated design/Single design, control unit-based design and integrated /multiplexer-based design [3]. The generalized block diagram for dedicated/single design architecture is as shown in Fig. 4. Other design approach which is popular among researcher for the flexibility to extend the design to incorporate additional operations is integrated design.

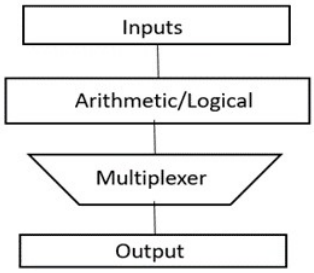

Fig. 4. Representation of the dedicated design

Integrated ALU approach involves in developing sub modules of the system individually and finally integrating them with the help of combinational circuit for choosing desired module. Block diagram of the integrated design is as presented in the Fig. 5.

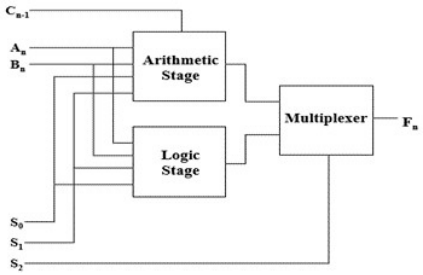

Fig. 5 Block diagram of the integrated design

Thomsen et al proposed first-ever ALU capable of performing 5 operations addition, subtraction, NOT, XOR and NOP. Two ALUs have been built by Y. Shymala and Tilak [9], but the design's prohibitive quantum cost means that it can perform at most a subset of those operations.

Matthew. M & Nagarajan. R [10] gave a novel design able to perform all the logical operations and arithmetic operations like addition and subtraction, however, the quantum cost and functionality of their design was not suitable for practical applications. Subhankar Pal, Chetan Vudadha [11] have successfully achieved 12 operations using NCV library, achieved the optimization of the cost metrics and architectural complexity. Kamaraj and Marichamy have proposed design through the usage of the novel gates designed [12]. 73 operations are realized by the dedicated deign ALU proposed by the authors S.Thakaral and D.Bhansal[13], but the functions realized through this architecture is redundant in nature and such design hardly ever finds application in the real time.

The multiplexer-based ALU layout is described in the study [14], and the logical unit and multiplexer layouts were both proved to work. To create a multiplexer based ALU, the author [15] turned to QCA (Quantum Cellular Automata) technology, namely the RM gate, which allowed for increased functionality with a sizeable garbage output and ancilla input. In the study [16], the authors present their ideas for ALU, which demonstrate enormous gains with respect to both cost metrics and simulation limitations. In [15], it was suggested that a reversible multiplexer may be used to create a testable reversible ALU unit. Reversible arithmetic and logic units (RLUs) are split off in the suggested ALU. These components are introduced independently, however the suggested ALU's QCA architecture is not detailed. Single-layer, circular cells are used in this design, and there are nine fixed inputs and fifteen additional outputs.

To create an ALU using fewer cells than conventional reversible gates, the unique suggested gates RG1, RG2, RG3, and RG4 were implemented. In [17], an ALU architecture is shown with a GN gate that has a large quantum cost and garbage, limiting the number of operations it can do to 8. In [19], the author has taken a more experimental approach to the architecture, increasing the ancilla input and quantum cost while decreasing trash output. By comparing them based on cost parameters of the reversible logic, the authors have attempted to optimise ALU circuit designs. Comparison of implemented ALU design in irreversible and reversible is carried out for 13 operations based on the power which doesn't convey much importance reversible logic [20].

More garbage and ancillary inputs imply less usefulness of reversible ALUs built using Toffoli gates [21]. Two reversible ALUs, one based on MRG gates and the other on HNG gates, are presented in [22]. These layouts are not adaptable and need higher garbage and ancillary lines for calculation. A programmable ALU based on Fredkin gates is presented in [23], however it has less input flexibility and more garbage outputs.

IV. PROPOSED DESIGN

In this paper proposed design is developed as dedicated ALU unit, capable of performing 22 operations with 5 selection lines. The multi-function unit implements standard arithmetic operations in digital computing, including add, subtract, carry, borrow, and increment/decrement. The logical operations are OR, AND, NOT, NAND, NOR XOR, XNOR, and buffer. It can perform 10 logical and 12 arithmetic operations. In the design proposed, Choice of the operation depends on the selection line S0, S1, S2 S3 and S5. Table I lists planned design operations.

Six reversible logic gates are used to form the design (see Fig. 6 for an illustration of the innovative suggested design), with four Fredkin gates, one Feynman gate, one SMG gate, and one HNG gate. Optimization of reversible logic parameters allows for cost estimation of the design. It is computed as 9 garbage outputs and the number of the input signals that are maintained at constant to balance the bijective of the reversible logic is 1. The total quantum cost involved in implementing the design is 28. Here A, B, and Cin are data inputs, and control inputs to choose the different operations are labeled as S1, S2, S3, S4, and S5.

TABLE I
PROPOSED DESIGN ALU OPERATIONS

S0	S1	S2	S3	S4	S5	Cin	Operation
0	0	0	1	0	0	0	OR
0	0	0	0	0	0	0	AND
0	0	0	1	1	0	0	NOR
0	0	0	0	1	0	0	NAND
0	1	0	1	0	1	0	XOR
1	0	1	0	0	1	1	XNOR
1	0	0	0	0	1	0	Buffer (A)
0	1	0	0	0	1	0	NOT of A
0	0	1	0	0	1	0	Buffer (B)
0	0	0	1	0	1	0	NOT of B
1	0	1	0	0	1	0	Add without Carry
1	0	1	0	0	1	1	Add with carry
1	0	0	0	0	1	1	Increment A
1	0	1	1	0	1	0	Decrement A
0	0	1	0	0	1	1	Increment B
1	1	1	0	0	1	0	Decrement B
1	0	0	1	0	1	0	A + B’
1	0	0	1	0	1	1	A + B’ + 1
0	1	1	0	0	1	0	A’ + B
0	1	1	0	0	1	1	A’+B’+1
0	1	1	0	1	1	0	Sub without carry
0	1	1	0	1	1	1	Sub with carry

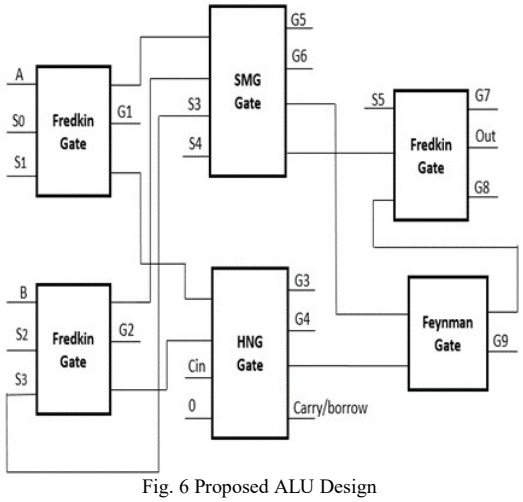

Fig. 6 Proposed ALU Design

V. RESULTS AND DISCUSSION

We have developed and tested the proposed design, as well as compared it to current options. The Xilinx Vivado tool is used to validate the design's functionality, while Verilog HDL is used to validate the design's structural level. Simulation results are tested for different combinations of data inputs A and B, as well for all the operations by applying different values for the selection inputs. Simulation results obtained for the proposed design is as illustrated in the Fig. 7 and Fig. 8.

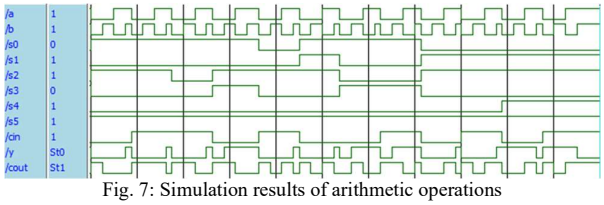

Fig. 7: Simulation results of arithmetic operations

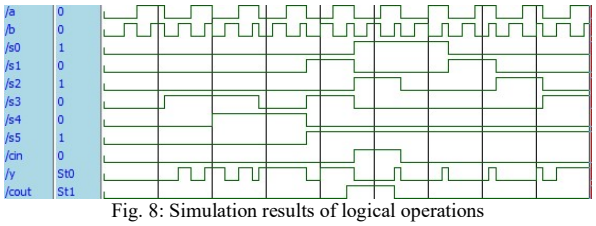

Fig. 8: Simulation results of logical operations

A final, RTL schematic representation of the suggested design is displayed in Fig. 9. The design is implemented on the FPGA Artix-7 series board and resource utilization in terms of the power and area usage is as shown in the Fig. 10.

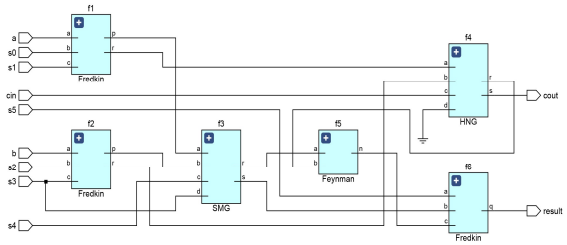

Fig.9 RTL Schematic of ALU Design

Power utilization is about 0.092w in which dynamic power is 0.001w and static power is 0.091w (as shown in, Fig. 10). Performance parameters of reversible logic as discussed in section 2.3 are used for comparing existing work with proposed one.

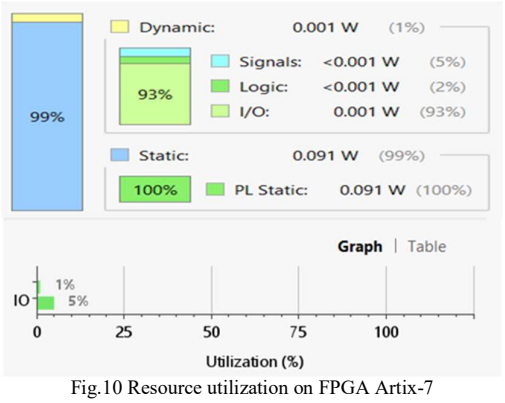

Fig.10 Resource utilization on FPGA Artix-7

It can be inferred from the table overall results analysed and observation reveals an improvement in the design proposed. Constant inputs reduced by 80% and 29%, respectively, in compared to previous work in [9] and [12]. and unwanted output is reduced by 57% comparing to with the work available in [12]. On other hand if the results were evaluated in terms of number of operations incorporated is found to be improved at average of 49% at per papers [9-14]. Fig. 11 gives graphical representation of this comparison.

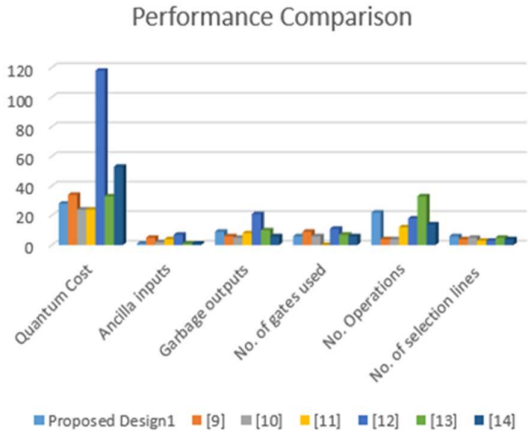

Fig. 11. Performance comparison of the proposed ALU

Table II consolidates the presented work with respect to the results of benchmark designs available in REVLIB repository. The number of operations achieved through present work is considerably more and quantum cost observed is also has reduced to greater extent. Despite the significant quantum cost, our results suggest that delay improvement is possible. While power consumption was calculated during algorithm verification, it was not tested after implementation in reversible logic since power consumption is zero during logical reversibility.

TABLE II
ANALYSIS OF THE SUGGESTED ARCHITECTURE IN REFERENCE TO REVLIB'S BENCHMARK CIRCUITS

Parameters	Prop. Design	ALU	ALU1	ALU2	ALU3	ALU4
Quantum Cost	28	114	228	5654	2632	55388
Ancilla inputs	1	0	8	6	8	8
Garbage outputs	9	4	12	10	10	14
No. of operations	22	8	8	6	8	8

VI. CONCLUSION

The fundamental objective of this research was to construct a reversible-logic ALU. Reversible gates are selected to assure reversible circuit desired is produced with least quantum cost. Performance evaluation of the dedicated ALU design is carried out to prove the improvement in the optimizing parameters. According to the findings of the research, the number of ancillary inputs has decreased by 50%, the amount of garbage output has decreased by 40%, and the propagation latency has decreased by 75%. We used FPGA to develop the approach, and then compared its area, latency, and power consumption. In spite of the fact that our methods resulted in a higher quantum cost in comparison to those of other methods that had been described before, it did not surpass the permissible limit.

REFERENCES

[1] R.Landauer, "Irreversibility and heat generation in the computing process", IBM J. Research and Development, Vol. 5, Issue. 3, pp.183-191, 1961. https://doi.org/10.1147/rd.53.0183

[2] C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, Vol. 17, Issue. 6, pp.525-532, 1973. https://doi.org/10.1147/rd.176.0525

[3] S. Girija, B. G. Sangeetha. "An Insight into the Existing Reversible Arithmetic and Logic Unit Designs", in Proceeding of Fifth International Conference on Microelectronics, Computing and Communication Systems, 2021. https://doi.org/10.1007/978-981-16-0275-7_32

[4] Subhankar Pal, Chetan Vudadha, Sai Phaneendra, Sreehari Veeramachaneni, Srinivas Mandalika, "A New Design of an n-bit Reversible Arithmetic Logic Unit", in Fifth International Symposium on Electronic System Design, pp.224-228, 2014. https://doi.org/10.1109/ISED.2014.56

[5] Zhijin Guan, Wenjuan Li, Weiping Ding, Yueqin Hang Lihui Ni, "An Arithmetic and Logic unit Design based on Reversible Logic", in Proceedings of 2011 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, 2011. https://doi.org/10.1109/PACRIM.2011.6033020

[6] M. K. Thomsen, R. G. Glück and H. B. Axelsen, "Reversible arithmetic logic unit for quantum arithmetic", Journal of Physics A: Mathematical and Theoretical", Vol. 43, Issue 43, pp. 217–230, 2010. https://doi.org/10.1088/1751-8113/43/38/382002

[7] Aprameya R S, Bhargavi N S, Karthik S, Girija S, "Optimized Reversible Arithmetic and Logic Unit (ALU)" International Journal of Engineering Research and Applications" Vol. 10, Issue 8, pp. 33-38, 2020. https://doi.org/10.9790/9622-1008053338

[8] Lenin Gopala, Nor Syahira Mohd M, K.Chowdhary, Alpha Agase Gopala, Ashutosh kumar Singh, "Design and synthesis of Reversible arithmetic and Logic Unit (ALU)", in IEEE International Conference on Control System, Computing and Engineering, pp.289- 293, 2014. https://doi.org/10.1109/I4CT.2014.6914191

[9] Y. Syamala and A. V. N. Tilak, "Reversible Arithmetic and Logic Unit", in 3rd International Conference on Electronics Computer Technology, pp. 207-211, 2011. https://doi.org/10.1109/ICECTECH.2011.5941987

[10] M. Matthew and Nagarajan. R, "Design of Reversible ALU on Novel Programmable Reversible Logic Gate structures", in International Conference on Electronics Computer Technology, pp.126-131, 2011. https://doi.org/10.1109/ISVLSI.2011.30

[11] A. Bolhassani and M. Haghparast, "Optimized Designs of Reversible Arithmetic Logic Unit," Turkish Journal of Electrical Engineering & Computer Sciences, Vol. 25, Issue. 2, pp. 1137-1146, 2017. https://doi.org/10.3906/elk-1505-223

[12] A.Kamaraj and P. Marichamy, "Design of Integrated Reversible Fault-Tolerant Arithmetic and Logic Unit", Microprocessors and Microsystems, Vol. 69, pp. 16-23, 2019. https://doi.org/10.1016/j.micpro.2019.05.009

[13] S.Thakral and D. Bansal, "Fault tolerant arithmetic logic unit", In: International Conference on Emerging Current Trends in Computing and Expert Technology, pp 226–233, 2019. https://doi.org/10.1007/978-3-030-32150-5_24

[14] Arindam Banerjee and Debesh Kumar Das, "A Novel ALU Circuit based on Reversible Logic", Journal of Circuits, Systems and Computers, Vol. 29, Issue. 11, pp. 1-17, 2020. https://doi.org/10.1142/S0218126620501728

[15] Bibhash Sen, Manojit Dutta, Mrinal Goswamia, Biplab K. Sikdar, "Modular Design of testable reversible ALU by QCA multiplexer with increase in programmability", Microelectronics Journal, Vol. 45, Issue. 11, pp 1522–1532, 2014. https://doi.org/10.1016/j.mejo.2014.08.012

[16] G.Kalita and Navajit Saikia, "Designing reversible arithmetic, logic circuit to implement micro-operation in quantum computation", in XXVII IUPAP Conference on Computational Physics (CCP2015), Vol. 759, pp. 1-6, 2016. https://doi.org/10.1088/1742-6596/759/1/012097

[17] A. Kamaraj and P. Marichamy, "Design and Implementation of Arithmetic and Logic Unit Using Novel Reversible Gates in Quantum Cellular Automata", in 4th International Conference on Advanced Computing and Communication Systems, pp. 1-6, 2017. https://doi.org/10.1109/ICACCS.2017.8014578

[18] Partha Khatter, Neeta Pandey, Kirti Gupta, "An Arithmetic and Logical Unit using Reversible Gates", in International Conference on Computing,

Power and Communication Technologies (GUCON), pp. 476-480, 2018. https://doi.org/10.1109/GUCON.2018.8675034

[19] Cissy Jose, T D Subash and, Simi P Thomas, "FPGA Implementation of dynamic Power, Area Optimized Reversible ALU For Various DSP Applications", Materials Today, Vol. 24, Issue. 3, pp. 2044-2053, 2020. https://doi.org/10.1016/j.matpr.2020.03.635

[20] S.Saniya Samrin, Rachamma Patil, Sumangala Itagi, Smita C Chetti, Afiya Tasneem, "Design of logic gates using reversible gates with reduced quantum cost", Global Transitions Proceedings, Vol. 3, pp. 136-141, 2022. https://doi.org/10.1016/j.gltp.2022.04.011

[21] Michael Kirkedal Thomsen, Robert Glück and Holger Bock Axelsen, "Reversible arithmetic logic unit for quantum arithmetic", Journal of Physics A: Mathematical and Theoretical, Vol. 43, Issue. 38, pp. 1-15, 2010. https://doi.org/10.1088/1751-8113/43/38/382002

[22] Safaiezadeh, B., Mahdipour, E., Haghparast, M. et al., "Novel design and simulation of reversible ALU in quantum dot cellular automata", J Supercomput, vol. 78, pp. 868–882, 2022. https://doi.org/10.1007/s11227-021-03860-y

[23] Morita, K., "Reversible Logic Gates. In: Theory of Reversible Computing. Monographs in Theoretical Computer Science", An EATCS Series. Springer, Tokyo. pp 77 – 101, 2017. https://doi.org/10.1007/978-4-431-56606-9_4